ATE Test Plan

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| Version | Author | Data | Comment |
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# Introduction

This document is the ATE production test plan. includes ARM, ETHERNET PHY, MIPHY, DDR3 PHY, PLL, Power-On-Reset IPs. This document includes test strategy, hardware requirement for ATE, description of test items.

Reliability tests, such as ESD, latch-up, life test etc are not covered.

|  |  |  |
| --- | --- | --- |
| Acronyms Introduction | | |
| Name | Full name | Description |
| ATE | Auto Test Equipment |  |
| WS | Wafer Sort |  |
| FT | Final Test |  |
| AWG | Analog Waveform Generator |  |
| DPS | Device Power Supply |  |
| DUT | Device Under Test | Die in the WS, packaged chip in the FT |
|  |  |  |

Table 1

# ATE Requirement

Device information:

|  |  |  |
| --- | --- | --- |
|  | Single Site  ( WS or FT ) | Multi-Site  ( WS or FT ) |
| Digital Channel |  |  |
| Power Supply: | VDD: digital 1.15v  VDDCA9: digital 1.15v  VDDCA9\_SOC: digital 1.15v  VDDQ: analog 1.5v/1.35v  VDD18: digital 1.8v  VDD33: digital 3.3v  AVDD25: analog 2.5v  HV: 7v for Fuse | VDD: digital 1.15v  VDDCA9: digital 1.15v  VDDCA9\_SOC: digital 1.15v  VDDQ: analog 1.5v/1.35v  VDD18: digital 1.8v  VDD33: digital 3.3v  AVDD25: analog 2.5v  HV: 7v for Fuse |
| Analog Module | NA | NA |

Table 2

Tester:

|  |  |
| --- | --- |
| specification | |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |

Table 3

Chip power [consum](javascript:void(0))ption:

|  |  |  |  |
| --- | --- | --- | --- |
| Power Name | current on each pad | pad quantity | total current |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

Table 4

Note:

1. Power consumption is based on power simulation of function pattern
2. PAD current is average current of total current

# Pad list

| **Pad Number** | **Pad Name** |
| --- | --- |
| **1** |  |
| 2 |  |
| 3 |  |
| 4 |  |
| 5 |  |
| 6 |  |
| 7 |  |
| 8 |  |
| 9 |  |
| 10 |  |
| **11** |  |
| 12 |  |
| 13 |  |
| 14 |  |
| 15 |  |
| 16 |  |
| 17 |  |
| 18 |  |
| 19 |  |
| 20 |  |
| 21 |  |
| 22 |  |
| 23 |  |
| 24 |  |
| 25 |  |
| 26 |  |
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| 28 |  |
| 29 |  |
| 30 |  |
| 31 |  |
| 32 |  |
| 33 |  |
| 34 |  |
| 35 |  |
| 36 |  |
| 37 |  |
| 38 |  |
| 39 |  |
| 40 |  |
| 41 |  |
| 42 |  |
| 43 |  |
| 44 |  |
| 45 |  |
| 46 |  |
| 47 |  |
| 48 |  |
| 49 |  |
| 50 |  |
| 51 |  |
| 52 |  |
| 53 |  |
| 54 |  |
| 55 |  |
| 56 |  |
| 57 |  |
| 58 |  |
| 59 |  |
| 60 |  |
| 61 |  |
| 62 |  |
| 63 |  |
| 64 |  |
| 65 |  |
| 66 |  |
| 67 |  |
| 68 |  |
| 69 |  |
| 70 |  |
| 71 |  |
| 72 |  |
| 73 |  |
| 74 |  |
| 75 |  |
| 76 |  |

Table 5

Digital Pad:

Power Pad:

GND Pad:

# Ball list

|  |  |  |
| --- | --- | --- |
| Ball NO. | Ball Name | Description |
| A1 |  |  |
| A2 |  |  |
| A3 |  |  |
| A4 |  |  |
| A5 |  |  |
| A6 |  |  |
| A7 |  |  |
| B1 |  |  |
| B2 |  |  |
| B3 |  |  |
| B4 |  |  |
| B5 |  |  |
| B6 |  |  |
| B7 |  |  |
| C1 |  |  |
| C2 |  |  |
| C3 |  |  |
| C4 |  |  |
| C5 |  |  |
| C6 |  |  |
| C7 |  |  |
| D1 |  |  |
| D2 |  |  |
| D3 |  |  |
| D4 |  |  |
| D5 |  |  |
| D6 |  |  |
| D7 |  |  |
| E1 |  |  |
| E2 |  |  |
| E3 |  |  |
| E4 |  |  |
| E5 |  |  |
| E6 |  |  |
| E7 |  |  |
| F1 |  |  |
| F2 |  |  |
| F3 |  |  |
| F4 |  |  |
| F5 |  |  |
| F6 |  |  |
| F7 |  |  |
| G1 |  |  |
| G2 |  |  |
| G3 |  |  |
| G4 |  |  |
| G5 |  |  |
| G6 |  |  |
| G7 |  |  |

Table 6

Total Ball:

Digital Ball:

Power Ball:

GND BALL:

# Test temperature and test sequence at WS and FT

## WS test sequence

## WS Test temperature is

|  |  |
| --- | --- |
|  | WS test item |
| 1 | DPS\_short |
| 2 | Continuity |
| 3 |  |
| 4 |  |
| 5 |  |
| 6 |  |
| 7 |  |
| 8 |  |
| 9 |  |
| 10 |  |
| 11 |  |
| 12 |  |
| 13 |  |
| 14 |  |
| 15 |  |
| 16 |  |
| 17 |  |
| 18 |  |
| 19 |  |
| 20 |  |
| 21 |  |
| 22 |  |
| 23 |  |
| 24 |  |
| 25 |  |
| 26 |  |
| 27 |  |
| 28 |  |
| 29 |  |
| 30 |  |
| 31 |  |
| 32 |  |

Table 7

**WS must use the wafer map from ST.**

## FT test sequence

## FT Test temperature is

|  |  |
| --- | --- |
|  | FT test item |
| 1 | DPS\_short |
| 2 | Continuity |
| 3 |  |
| 4 |  |
| 5 |  |
| 6 |  |
| 7 |  |
| 8 |  |
| 9 |  |
| 10 |  |
| 11 |  |
| 12 |  |
| 13 |  |
| 14 |  |
| 15 |  |
| 16 |  |
| 17 |  |
| 18 |  |
| 19 |  |
| 20 |  |
| 21 |  |
| 22 |  |
| 23 |  |
| 24 |  |
| 25 |  |
| 26 |  |
| 27 |  |
| 28 |  |
| 29 |  |
| 30 |  |
| 31 |  |
| 32 |  |

Table 8

# ATE test program development and release procedure.

(1) According to the test request and spec from designer and end customer, create the test plan. After getting designer and end customer's confirm, release the test plan

(2) Test program debugging. Provide the test result to the designer and the end customer to review and discuss. Then determine the final test condition, sequence and limit. Then update the test plan.

(3) Release Test program according to VSI's standard test program release procedure.

(4) Monitor the yield of the first production lots, and analyze the failed units to improve the test program. Update the test plan.

# Test Description

TEST MODE:

|  |  |  |
| --- | --- | --- |
| **MODE NAME** | **TESTMODE** | **TEST\_MODES\_IDENTIFY\_PIN\_SETS** |
| Function | 0 | Don’t care |
| SoC Top SCAN mode | 1 | {000000} |
| Switch block SCAN mode | 1 | {000001} |
| A9SS block SCAN mode | 1 | {000010} |
| 5 EPHY INTEST SCAN mode | 1 | {010001} |
| 2 PCIe MiPHY INTEST SCAN mode | 1 | {010010} |
| 4 Switch MiPHY INTEST SCAN mode | 1 | {010011} |
| MBIST mode | 1 | {000011} |
| BSD mode | 1 | {010000} |
| A9SS PLL BIST mode | 1 | {001000} |
| EFUSE mode | 1 | {000100} |
| VT sensor calibration mode | 1 | {000101} |
| PMB sensor external control mode | 1 | {000110} |
| DDR PHY test mode | 1 | {000111} |
| PCIe MiPHY test mode | 1 | {001001} |
| Switch MiPHY0 test mode | 1 | {001010} |
| Switch MiPHY1 test mode | 1 | {001011} |
| Switch MiPHY2 test mode | 1 | {001100} |
| Switch MiPHY3 test mode | 1 | {001101} |
| GMAC EPHY test mode | 1 | {001110} |
| Switch 4 EPHY test mode | 1 | {001111} |
|  |  |  |

Table 9

## Continuity

|  |  |  |  |
| --- | --- | --- | --- |
| Continuity Test Condition | | | |
| No. | item | value | Unit |
| 1 | Test frequency | NA | MHZ |
| 2 |  | 0 | V |
| 3 |  | 0 | V |
| 4 |  | 0 | V |

Table 10

**Test Methods:**

Connect all device power supply pins to VSS.

Connect all signal pins to PMU and force -100uA current on individual signal pins.

**Measure Pins:**

All digital inputs, IOs, Outputs.

Limit: -200~-800mv



Diagram 1

Measure Diode to GND

## DPS Short

|  |  |  |  |
| --- | --- | --- | --- |
| DPS Short Test Condition | | | |
| No. | item | value | Unit |
| 1 | Test frequency | NA | MHZ |
| 2 |  | 0.1 | V |
| 3 |  | 0.1 | v |
| 4 |  | 0.1 | v |

Table 11

**Test Methods:**

Add 100 mV voltages on DPS pin and measure DPS current, prevent short current flow and protect test hardware.

Test Limit: according to actual result

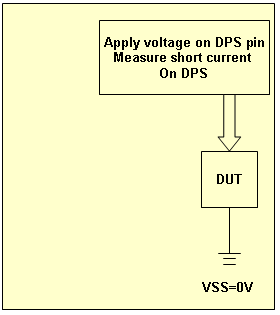


Diagram 2

## Input leakage test

|  |  |  |  |
| --- | --- | --- | --- |
| Leakage Test Condition | | | |
| No. | item | value | unit |
| 1 | Test frequency | NA | MHZ |
| 2 |  |  | v |
| 3 |  |  | v |
| 4 |  |  | v |

Table 13

**Input Leakage Low**

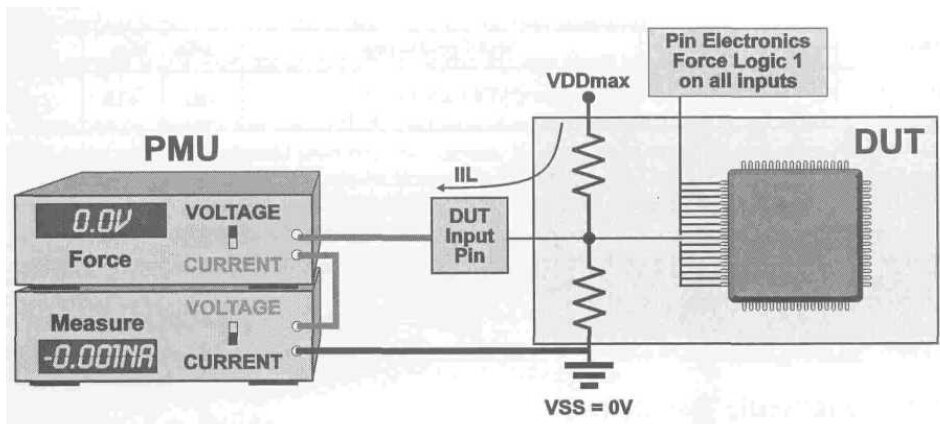


Diagram 3

**Input Leakage High**

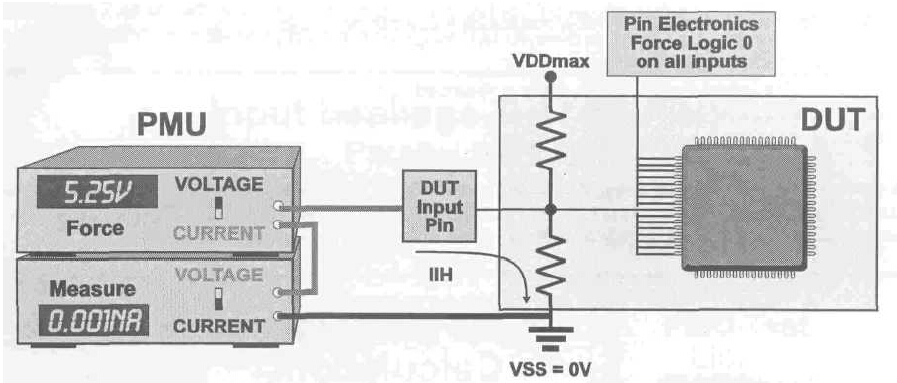


Diagram 4

**Test Methods:**

Power on chip, run test pattern to set all bidirectional pins into input mode, and disable output, force 1.98v(3.63v)/0v voltage on input and output pins, measure leakage current.

Test pattern: set all bidirectional pins into input mode。

Test limit:

## Pull Up/Pull Down Test

|  |  |  |  |
| --- | --- | --- | --- |
| Pull Up/Down Test Condition | | | |
| No. | item | value | unit |
| 1 | Test frequency | NA | MHZ |
| 2 |  |  | v |
| 3 |  |  | v |
| 4 |  |  | v |

Table 14

**Pull-up:**

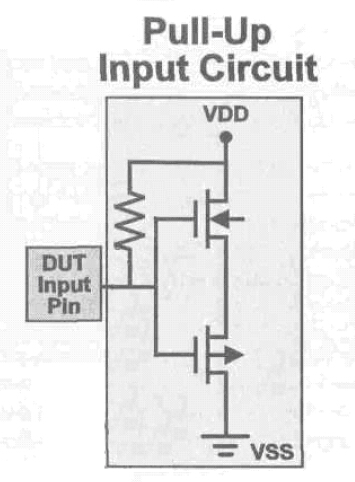


Diagram 5

**Pull-down:**

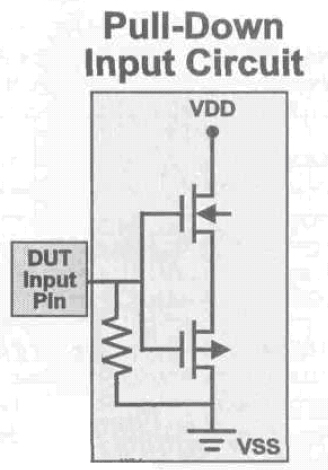


Diagram 6

**Test Methods:**

Power on chip, force 0V voltage on pull up pins, measure pull-up current.

Power on chip, force the same voltage as VDDIO on pull down pins, measure pull-down current.

Be attention: pull-up/down test can only be execute in function mode.

Test limit: according to the IO spec

**Pull up/down pin list:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | Pin Name | IO type | Pull down/up |
| 1 |  |  |  |
| 2 |  |  |  |
| 3 |  |  |  |
| 4 |  |  |  |
| 5 |  |  |  |
| 6 |  |  |  |

Table 15

## BSD Test

|  |  |  |
| --- | --- | --- |
| Boundary Scan mode | | |
| IO port name | direction | description |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

Table 16

|  |  |  |  |
| --- | --- | --- | --- |
| BSD Test Condition | | | |
| No. | item | value | unit |
| 1 | Test frequency |  | MHZ |
| 2 |  |  | v |
| 3 |  |  | v |
| 4 |  |  | v |

Table 17

**Test Methods:**

Run BSD pattern to check the function of digital input/output pins

For 3.3v IO

VOH: 2.31v

VOL: 0.99v

Test pattern:

## VIH/VIL/VOH/VOL test

### VIH/VIL test

|  |  |  |  |
| --- | --- | --- | --- |
| VIH/VIL/VOH/VOL Test Condition | | | |
| No. | item | value | unit |
| 1 | Test frequency |  | MHZ |
| 2 |  |  | v |
| 3 |  |  | v |
| 4 |  |  | v |

Table 18

**Test Methods:**

For 3.3v IO:

Input VDDIO\*70% as “1” and VDDIO\*30% as “0” to input pins, run the test pattern, check the output is correct or not.

DPS voltage: 2.97v/3.63v

Test limit:

VOH:

VOL:

**Input pin list**

| No. | Pin name | Direction | Schmitt | Input Condition |
| --- | --- | --- | --- | --- |
| 1 |  |  | NO | VIH: VDDIO\*70%  VIL: VDDIO\*30% |
| 2 |  |  |
| 3 |  |  |
| 4 |  |  |
| 5 |  |  |
| 6 |  |  |
| 7 |  |  |
| 8 |  |  |
| 9 |  |  |
| 10 |  |  |
| 11 |  |  |
| 12 |  |  |
| 13 |  |  |
| 14 |  |  |
| 15 |  |  |
| 16 |  |  |
| 17 |  |  |
| 18 |  |  |
| 19 |  |  |
| 20 |  |  |
| 21 |  |  |
| 22 |  |  | YES | VIH: VDDIO\*70IO VIL: VDDIO\*30% |
| 23 |  |  |

Table 19

### VOH/VOL test

**Test Methods:**

For 3.3v IO:

Input VDDIO voltage as “1” and 0v as “0” to input pins, run the test pattern, add current loads on output pins, and check VOH/VOL level of the output is correct or not.

DPS voltage:

Test limit:

VOH:

VOL:

| No. | Pin name | Current load |
| --- | --- | --- |
| 1 |  |  |
| 2 |  |  |
| 3 |  |  |
| 4 |  |  |
| 5 |  |  |
| 6 |  |  |
| 7 |  |  |
| 8 |  |  |
| 9 |  |  |
| 10 |  |  |
| 11 |  |  |

Table 20

Test pattern:

## SCAN DC and AC Test

SCAN configuration

|  |  |
| --- | --- |
| **Constraints** | **Values** |
| Scan model | Internal & compression |
| Scan style | Multiplexed flip-flop |
| Scan registers Number | 380384( include ddrphy ~30000) |
| Scan chain count | 57 |
| Clock mixing | yes |
| Compress ratio | 35 |

SOC SCAN test Pads distribution table

|  |  |  |  |
| --- | --- | --- | --- |
| **Scan Ports** | **Port Dir** | **Port Type** | **Chain length** |
| CLOCKREC0\_OUT | INPUT | Test clock |  |
| M1\_LED\_LINK | INPUT | Ate clock |  |
| RESETCHIP | INPUT | Test reset |  |
| CLOCKREC0\_VALID | INPUT | Scan enable |  |
| CLOCKCORE | INPUT | Ref\_clk1 |  |
| CLOCKSERDES | INPUT | Ref\_clk2 |  |
| M0\_LED\_LINK | INPUT | Scan\_compress |  |
| M2\_LED\_LINK | INPUT | Pll\_reset |  |
| M3\_LED\_LINK | INPUT | Pll\_bypass |  |
| LB\_RDDATA[0] | INPUT | Scan\_in0 | ~7000 |
| LB\_RDDATA[1] | INPUT | Scan\_in1 | ~7000 |
| LB\_RDDATA[2] | INPUT | Scan\_in2 | ~7000 |
| LB\_RDDATA[3] | INPUT | Scan\_in3 | ~7000 |
| LB\_RDDATA[4] | INPUT | Scan\_in4 | ~7000 |
| LB\_RDDATA[5] | INPUT | Scan\_in5 | ~7000 |
| LB\_RDDATA[6] | INPUT | Scan\_in6 | ~7000 |
| LB\_RDDATA[7] | INPUT | Scan\_in7 | ~7000 |
| LB\_RDDATA[8] | INPUT | Scan\_in8 | ~7000 |
| LB\_RDDATA[9] | INPUT | Scan\_in9 | ~7000 |
| LB\_RDDATA[10] | INPUT | Scan\_in10 | ~7000 |
| LB\_RDDATA[11] | INPUT | Scan\_in11 | ~7000 |
| LB\_RDDATA[12] | INPUT | Scan\_in12 | ~7000 |
| LB\_RDDATA[13] | INPUT | Scan\_in13 | ~7000 |
| LB\_RDDATA[14] | INPUT | Scan\_in14 | ~7000 |
| LB\_RDDATA[15] | INPUT | Scan\_in15 | ~7000 |
| LB\_ADDR[0] | INPUT | Scan\_in16 | ~7000 |
| LB\_ADDR[1] | INPUT | Scan\_in17 | ~7000 |
| LB\_ADDR[2] | INPUT | Scan\_in18 | ~7000 |
| LB\_ADDR[3] | INPUT | Scan\_in19 | ~7000 |
| LB\_ADDR[4] | INPUT | Scan\_in20 | ~7000 |
| LB\_ADDR[5] | INPUT | Scan\_in21 | ~7000 |
| LB\_ADDR[6] | INPUT | Scan\_in22 | ~7000 |
| LB\_ADDR[7] | INPUT | Scan\_in23 | ~7000 |
| LB\_ADDR[8] | INPUT | Scan\_in24 | ~7000 |
| LB\_ADDR[9] | INPUT | Scan\_in25 | ~7000 |
| LB\_ADDR[10] | INPUT | Scan\_in26 | ~7000 |
| LB\_ADDR[11] | INPUT | Scan\_in27 | ~7000 |
| LB\_ADDR[12] | INPUT | Scan\_in28 | ~7000 |
| LB\_ADDR[13] | INPUT | Scan\_in29 | ~7000 |
| LB\_ADDR[14] | INPUT | Scan\_in30 | ~7000 |
| LB\_ADDR[15] | INPUT | Scan\_in31 | ~7000 |
| LB\_ADDR[16] | INPUT | Scan\_in32 | ~7000 |
| LB\_ADDR[17] | INPUT | Scan\_in33 | ~7000 |
| LB\_ADDR[18] | INPUT | Scan\_in34 | ~7000 |
| LB\_ADDR[19] | INPUT | Scan\_in35 | ~7000 |
| LB\_ADDR[20] | INPUT | Scan\_in36 | ~7000 |
| LB\_CS[0] | INPUT | Scan\_in37 | ~7000 |
| LB\_CS[1] | INPUT | Scan\_in38 | ~7000 |
| LB\_CS[2] | INPUT | Scan\_in39 | ~7000 |
| LB\_RD | INPUT | Scan\_in40 | ~7000 |
| QSPI\_DIO0 | INPUT | Scan\_in41 | ~7000 |
| QSPI\_DIO1 | INPUT | Scan\_in42 | ~7000 |
| QSPI\_DIO2 | INPUT | Scan\_in43 | ~7000 |
| QSPI\_DIO3 | INPUT | Scan\_in44 | ~7000 |
| GPIO39 | INPUT | Scan\_in45 | ~7000 |
| GPIO38 | INPUT | Scan\_in46 | ~7000 |
| GPIO0 | INPUT | Scan\_in47 | ~7000 |
| GPIO1 | INPUT | Scan\_in48 | ~7000 |
| GPIO2 | INPUT | Scan\_in49 | ~7000 |
| CTRL\_PIN0 | INPUT | Scan\_in50 | ~7000 |
| CTRL\_PIN1 | INPUT | Scan\_in51 | ~7000 |
| CTRL\_PIN2 | INPUT | Scan\_in52 | ~7000 |
| CTRL\_PIN3 | INPUT | Scan\_in53 | ~7000 |
| CMTOD\_ONEPPSI | INPUT | Scan\_in54 | ~7000 |
| CMTOD\_TODI | INPUT | Scan\_in55 | ~7000 |
| E0\_LED\_LINK | INPUT | Scan\_in56 | ~7000 |
| LB\_DATA[0] | OUTPUT | Scan\_out0 | ~7000 |
| LB\_DATA[1] | OUTPUT | Scan\_out1 | ~7000 |
| LB\_DATA[2] | OUTPUT | Scan\_out2 | ~7000 |
| LB\_DATA[3] | OUTPUT | Scan\_out3 | ~7000 |
| LB\_DATA[4] | OUTPUT | Scan\_out4 | ~7000 |
| LB\_DATA[5] | OUTPUT | Scan\_out5 | ~7000 |
| LB\_DATA[6] | OUTPUT | Scan\_out6 | ~7000 |
| LB\_DATA[7] | OUTPUT | Scan\_out7 | ~7000 |
| LB\_DATA[8] | OUTPUT | Scan\_out8 | ~7000 |
| LB\_DATA[9] | OUTPUT | Scan\_out9 | ~7000 |
| LB\_DATA[10] | OUTPUT | Scan\_out10 | ~7000 |
| LB\_DATA[11] | OUTPUT | Scan\_out11 | ~7000 |
| LB\_DATA[12] | OUTPUT | Scan\_out12 | ~7000 |
| LB\_DATA[13] | OUTPUT | Scan\_out13 | ~7000 |
| LB\_DATA[14] | OUTPUT | Scan\_out14 | ~7000 |
| LB\_DATA[15] | OUTPUT | Scan\_out15 | ~7000 |
| LB\_ADDR\_ERR | OUTPUT | Scan\_out16 | ~7000 |
| LB\_OPR\_ACK | OUTPUT | Scan\_out17 | ~7000 |
| LB\_CLOCK\_OUT | OUTPUT | Scan\_out18 | ~7000 |
| SNF\_SCK | OUTPUT | Scan\_out19 | ~7000 |
| SNF\_CS | OUTPUT | Scan\_out20 | ~7000 |
| SNF\_SI | OUTPUT | Scan\_out21 | ~7000 |
| SNF\_SO | OUTPUT | Scan\_out22 | ~7000 |
| SNF\_HOLD | OUTPUT | Scan\_out23 | ~7000 |
| SNF\_WP | OUTPUT | Scan\_out24 | ~7000 |
| UART0\_RX | OUTPUT | Scan\_out25 | ~7000 |
| UART0\_TX | OUTPUT | Scan\_out26 | ~7000 |
| UART1\_RX | OUTPUT | Scan\_out27 | ~7000 |
| UART1\_TX | OUTPUT | Scan\_out28 | ~7000 |
| JTAG0\_TCK | OUTPUT | Scan\_out29 | ~7000 |
| JTAG0\_TDI | OUTPUT | Scan\_out30 | ~7000 |
| JTAG0\_TDO | OUTPUT | Scan\_out31 | ~7000 |
| JTAG0\_TMS | OUTPUT | Scan\_out32 | ~7000 |
| JTAG1\_TCK | OUTPUT | Scan\_out33 | ~7000 |
| JTAG1\_TDI | OUTPUT | Scan\_out34 | ~7000 |
| JTAG1\_TDO | OUTPUT | Scan\_out35 | ~7000 |
| JTAG1\_TMS | OUTPUT | Scan\_out36 | ~7000 |
| JTAG1\_TRST | OUTPUT | Scan\_out37 | ~7000 |
| I2C\_SCL0 | OUTPUT | Scan\_out38 | ~7000 |
| I2C\_SDC0 | OUTPUT | Scan\_out39 | ~7000 |
| I2C\_SCL1 | OUTPUT | Scan\_out40 | ~7000 |
| I2C\_SDC1 | OUTPUT | Scan\_out41 | ~7000 |
| I2C\_SCL2 | OUTPUT | Scan\_out42 | ~7000 |
| I2C\_SDC2 | OUTPUT | Scan\_out43 | ~7000 |
| I2C\_SCL3 | OUTPUT | Scan\_out44 | ~7000 |
| I2C\_SDC3 | OUTPUT | Scan\_out45 | ~7000 |
| I2C\_SCL4 | OUTPUT | Scan\_out46 | ~7000 |
| I2C\_SDC4 | OUTPUT | Scan\_out47 | ~7000 |
| INTERRUPT0 | OUTPUT | Scan\_out48 | ~7000 |
| INTERRUPT1 | OUTPUT | Scan\_out49 | ~7000 |
| SPI\_SCLK | OUTPUT | Scan\_out50 | ~7000 |
| SPI\_CS | OUTPUT | Scan\_out51 | ~7000 |
| SPI\_SDI | OUTPUT | Scan\_out52 | ~7000 |
| SPI\_SDO | OUTPUT | Scan\_out53 | ~7000 |
| WDT\_INTERRUPT | OUTPUT | Scan\_out54 | ~7000 |
| QSPI\_CLK | OUTPUT | Scan\_out55 | ~7000 |
| QSPI\_CS | OUTPUT | Scan\_out56 | ~7000 |

Table 21

|  |  |  |  |
| --- | --- | --- | --- |
| SCAN Test Condition | | | |
| No. | item | value | unit |
| 1 | SCAN DC test frequency |  | MHZ |
| 2 | SCAN DC test frequency |  | MHZ |
| 3 |  |  | v |
| 4 |  |  | v |
| 5 |  |  | v |

Table 22

SCAN DC test fault coverage:

SCAN AC test fault coverage:

SCAN DC frequency:

SCAN AC frequency:

Test limit:

For 3.3v IO

VOH: 2.31v

VOL: 0.99v

Test pattern:

## MBIST Test

|  |  |  |
| --- | --- | --- |
| MBIST Mode | | |
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Table 23

**Total 7 memory instances:**

|  |  |  |  |
| --- | --- | --- | --- |
| Instance name | Words num | Bits num | type |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
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|  |  |  |  |

Table 24

MBIST Algorithms:

-- March1

-- March2

-- RetentionCB

-- addressdecode\_bg0

-- addressdecode\_bg1

|  |  |  |  |
| --- | --- | --- | --- |
| MBIST Test Condition | | | |
| No. | item | value | unit |
| 1 | Test frequency | 40 | MHZ |
| 2 |  |  | v |
| 3 |  |  | v |
| 4 |  |  | v |

Table 25

Run MBIST pattern to test the RAM.

Test limit:

For 3.3v IO

VOH: 2.31v

VOL: 0.99v

Test pattern:

## MiPHY Test

Test Items Table

|  |  |  |  |
| --- | --- | --- | --- |
| Description | Min voltage | Nom voltage | Max voltage |
| Init pci/sgmii | Y | Y | Y |
| Osc test |  | Y |  |
| Frequency test |  | Y |  |
| SSC frequency test |  | Y |  |
| PLL test |  | Y |  |
| PCI/SGMII bist, max. genX, internal loopback with SSCOFF | Y | Y | Y |
| PCI/SGMII bist, gen1,external loopback with SSCOFF |  | Y |  |
| PCI/SGMII bist, max. genX, external loopback with SSCOFF | Y |  |  |
| PCI/SGMII bist, max. genX, external loopback with SSCON | Y |  |  |
| PCI/SGMII bist, max. genX, external loopback with SSCON, frequency +5% | Y |  |  |
| PCI/SGMII bist, max. genX, external loopback with SSCOFF, only pre-emphasis bytes | Y |  |  |
| EOM test(Eye Opening Margin) |  | Y |  |
| **DC test** | | | |
| TX supply test |  | Y |  |
| TX swing test |  | Y |  |
| TX/RX common mode test |  | Y |  |
| TX/RX impedance test |  | Y |  |
| **AC test** | | | |
| Sigdet at speed test |  | Y |  |
| Sigdet with beacon lfps test |  | Y |  |
| TX send beacon lfps test |  | Y |  |
| Txdetectrx test |  | Y |  |

### AC Test

1. Initialization test

(1) Test method: run test pattern to check the digital output

(2) Test pattern is provided By Fiberhome

2. Oscillator test

(1) ST/Fiberhome should provide the detial test method

3. Frequency test

(1) Test method: Run pattern and measure the frequency

4. PLL test

(1) Test method: Run pattern and measure the TX output frequency

5. BIST test

(1) Test method: Run pattern to do internal loopback test

Run pattern to do external loopback test

BIST loopback modes

ATE Final Test Board Scheme

Recommended values for AC coupling capacitors between TX and RX are:

For SATA: 12nF

For PCIe: 75 to 200nF

For USB3: 75 to 200nF

Be attention that, refres pin need to connect a relay to switch for 3 connections:

* Refres connects to vdd\_pll through a 487ohms resistor
* Refres connects to vdd\_pll directly
* Refres connects to digital ATE digital channel

ATE WS Board Scheme

6. EOM test

(1) Run pattern to do EOM test

EOM test configuration

7.Sigdet at speed test

(1) Test Purpose:

The Sigdet at speed (signal detect) uses the TX buffer programmable swing feature to provide input data to the RX buffer though an external loopback path. This allows the Phy signal-detect function to be tested without using an external arbitrary waveform generator.

(2) Test method:

* Initialize the Phy
* Program TX buffer swing to 50mv VPP
* Launch external bist
* Check sigdet\_db is 0
* Program TX buffer swing to 400mv VPP
* Launch external bist
* Check sigdet\_db is 1

port-to-port signal detect test configuration

8. Sigdet with beaconlfps test

(1) Test Purpose:

The Sigdet with beaconlfps test uses the TX buffer programmable swing feature to provide input data to the RX buffer though an external loopback path. The generated signal is a beacon or LFPS pattern. This pattern is a low frequency pattern(reference clock frequency) used by PCIE standard (beacon).

(2) Test Method:

* Initialize the Phy
* Program TX buffer swing to 50mv VPP
* Launch beacon/lfps pattern
* Check sigdet\_trigger\_fds is 0
* Check sigdet\_fds is 0(or px\_sigdet)
* Program TX buffer swing to 400mv VPP
* Check sigdet\_trigger\_fds is 1
* Check sigdet\_fds is 1(or px\_sigdet)

9. TX send beacon lfps test

(1) Test Purpose:

The TX send beacon LFPS test checks that the PHY deserializer and TX buffer can transmit a beacon and LFPS signal at the correct frequency using the send-beacon function.

(2) Test method:

* Initialize the Phy
* Activate MiPHY send beacon/lfps function to send a clock pattern on the px\_txp/px\_txn outputs(dependent on clock oscillator)
* Measure the frequency on px\_txp/px\_txn.

TX idle mode test hardware configuration

10 TX detect RX test

(1) Test Purpose:

The TX detect RX comparator test verifies that a load is detected when an RX differential input buffer is connected to the TX differential outputs.

(2) Test Method:

* Initialize the Phy
* Set power Phy mode to operative mode 2
* Perform the following for polarity 0(negative pulse) and 1(positive pulse)

1. close the loopback to connect TX to RX
2. check TXdetectRX out
3. send the pulse
4. check TXdetectRX out

* Perform the following for polarity 0(negative pulse) and 1(positive pulse)

1. open the loopback to connect the ATE to the TX
2. disconnect all TX branches(tx output internal floating)
3. apply from the ATE to TXP and TXN a DC level below and above TX detect RX block threshold

### DC Test

1. Supply Test

(1) Test Purpose:

This test measures the internal supply level present on the IO, it's just required on characterization and not needed on production test.

(2) Test method:

Run pattern to initialize the Phy, program the power rail for each measurement, then measure the voltage level for each case.

2. TX Supply test

(1) Test Purpose:

The unloaded TX buffer output voltage indicates the TX regulator supply level. Its measurement checks the regulator voltage and the internal reference function.

(2) Test Method:

* Run pattern to initialize the MiPHY IP
* Program the test word to generate a DC level (txp=1, txn=0)
* Program TX branch to force only single branches (not differential)
* Execute the measurement of Vtxp-Vtxn

TX buffer supply level test configuration

(3) Test limit:

It's needed to be provided by Fiberhome/ST.

3. TX Swing test

(1) Test Purpose:

This test checks that the serial output buffer pins px\_txp and px\_txn are capable of driving the specified DC levels.

(2) Test Method:

Run pattern to program the TX output differential DC voltage level 0 and 1, measure the txp and txn, calculate the Vdiff and Vcommon.

(3) Test Limit:

It's needed to be provided by Fiberhome/ST.

4. TX/RX common mode test

(1) Test Purpose:

This test verifies TX and RX common mode. Each single-ended input px\_rxp/px\_rpn can be considered as DC terminated to a bias voltage through a compensated 50-ohm resistor.

(2) Test Method:

* Run pattern to initialize the Phy and put the TX in idle mode
* Measure TX output common mode Vm1 and Vm2. (Vm1=Vm2=Vdd/2)
* Measure default RX input common mode voltage with different settings

TX idle mode test configuration

RX bias test configuration

(3) Test Limit:

It's needed to be provided by customer

5. TX/RX impedance test

(1) Test Purpose:

The TX output impedance against Rref test verifies the compensated output resistance of the TX buffer when the Phy is in operating mode.

The RX input impedance against Rref test verifies the compensated output resistance of the RX buffer when the Phy is in operating mode.

(2) Test Method:

① TX common-mode output impedance test configuration

* Initialize the Phy(no differential 100ohm load)
* Set the TX block into idle mode
* Measure TX idle common mode voltage: Vtxidle
* Force +0.5mA on px\_txp and px\_txn, measure Vtxp and Vtxn
* Calculate common-mode impedance: Ztxcm=(Vtxp+Vtxn-2\* Vtxidle)/2\*10-3

② TX differential output impedance test configuration

* Plug 100 ohms load
* The TX is put in normal mode generating a static test word(TXP=1,TXN=0) to execute differential impedance measurement
* Measure TX default differential output voltage Vout.
* Vtxsupplylevel is measured by TX supply test item. Calculate differential impedance: Ztx=100\*(Vtxsupplylevel-Vout)/Vout
* Set other modes(offset+1, offset-1, minimum com\_tx code, maximum minimum com\_tx code) , repeat above steps and calculate the impedance of different modes.

③RX impedance test configuration

* Set RX into reset mode, force +5uA on RXP and RXN, measure the voltage: Vrxp and Vrxn. Calculate the Common-mode impedance under reset:

Zrxcm\_reset=(Vrxp+Vrxn)/20\*10-6

* Set RX into normal mode, force +0.5mA on RXP and RXN, measure the voltage: Vrxp and Vrxn. Calculate the Common-mode impedance:

Zrxcm=(Vrxp+Vrxn-2\*Vrxbias)/20\*10-3

* Set RX into differential default mode, force +0.5mA on RXP and -0.5mA on RXN, measure the voltage: Vrxp and Vrxn. Calculate the differential impedance:

Zrx=(Vrxp+Vrxn)/0.5\*10-3

* Set RX into differential other modes(comp+1,comp-1, maximum comp\_rx, minimum comp\_ex), force +0.5mA on RXP and -0.5mA on RXN, measure the voltage: Vrxp and Vrxn. Calculate the differential impedance:

Zrx=(Vrxp+Vrxn)/0.5\*10-3

* Put Refres= infinite(disconnect), read comp\_tx and comp\_rx codes
* Put Refres= 0(short), read comp\_tx and comp\_rx codes

## Power On Reset Test

|  |  |  |
| --- | --- | --- |
| Analog Test Mode | | |
| pin name | direction | description |
|  |  |  |
|  |  |  |
|  |  |  |
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Table 34

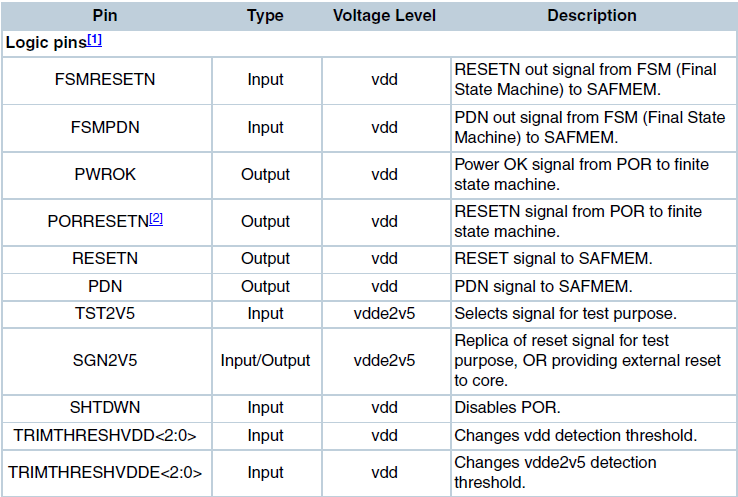
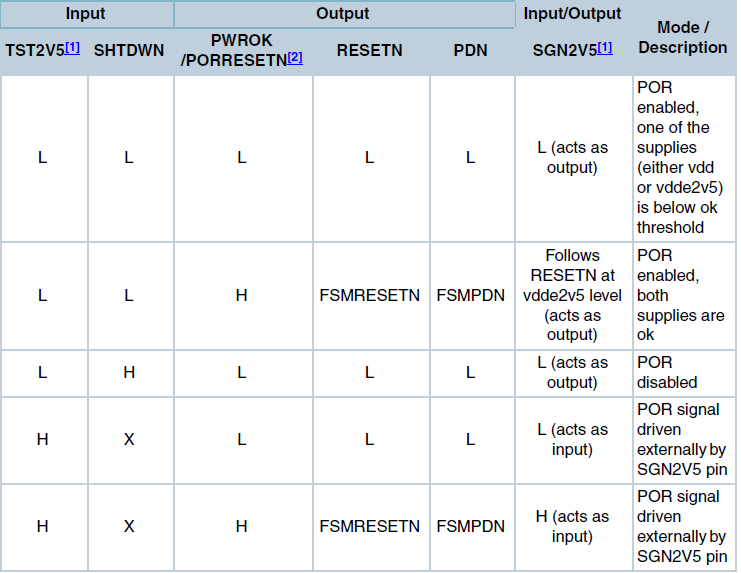


Table 35

True Table



(1) Test Purpose:

To test POR function and the delay time between PWROK and PORRESETN.

(2) Test Method:

① Power on vdd and vdde2v5, set vdd=1v and vdde25=2.25v

② Check that if the output of PWROK and PORRESETN become high or not, and PORRESETN rising edge delayed 20uS after PWROK rising edge.

③ Set TRIMTHRESVDD[2:0] and TRIMTHRESVDDE[2:0] to different value, also power on vdd and vdde2v5 to different level to check the POR function

Threshold Selection for Vdd Supply detection

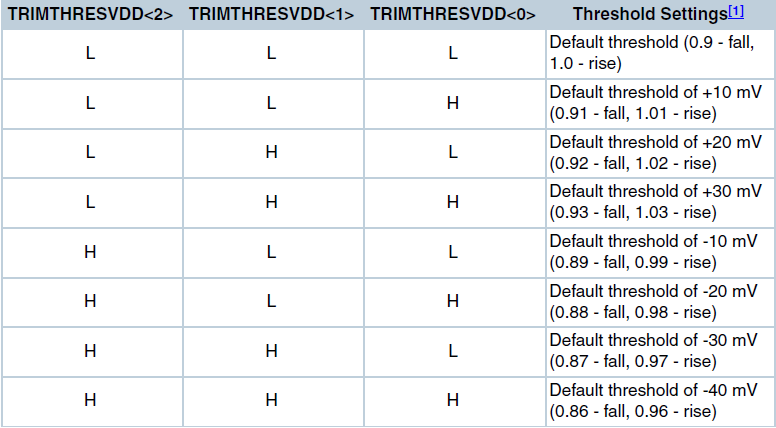
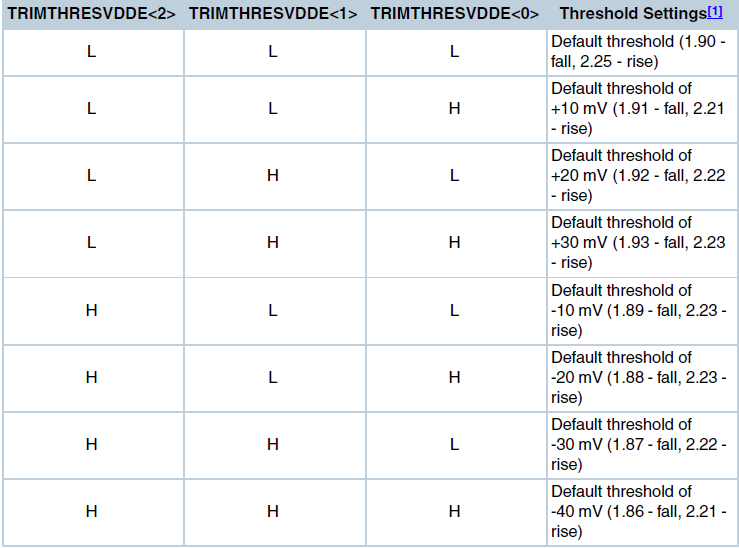


Table 36

Threshold Selection for Vdde2v5 Supply detection



## DDR PHY Test

1. DDL Test

(1) Test Purpose:

Test multiple embedded DLLs of DDL

(2) Test Method:

Run Pattern to check DDL

2. PLL Test

(1) Test Purpose:

Measure the output frequency of PLL.

(2) Test Method:

Run Pattern to set the PLL, and measure the output frequency.

3. SSTL IO Test

These test items(VIH/VIL/VOH/VOL, input/output impedance) will be included in BSD and VIH/VIL/VOH/VOL tests.

Appendix A: reference files